In the Claims

59. (New) An imaging device, comprising:

a photosensitive device for accumulating photo-generated charge having a generally S-shaped active area contacting a column output line in an underlying portion of a semiconductor substrate; and

a readout circuit comprising at least an output transistor;

wherein said imaging device is in a row of similar imaging devices in an array and shares said column output line with an adjacent imaging device of the row.

60. (New) The imaging device according to claim 59, wherein said photosensitive device is one of a photogate, a photodiode or a photoconductor.

61. (New) The imaging device according to claim 59, further comprising a controllable charge transfer region having a control terminal, said transfer region being formed in said substrate adjacent said active area and having a node connected to a gate of said output transistor and at least one charge transfer device for transferring charge from said active area to said node in accordance with a control signal applied to said control terminal.

62. (New) The imaging device according to claim 61, wherein said charge transfer device is a field effect transistor.

63. (New) The imaging device according to claim 59, further comprising a straight column line formed of a metal layer in an integrated circuit to address said imaging device.

64. (New) The imaging device according to claim 59, further comprising a reset transistor for resetting said node in response to a reset signal.

65. (New) The imaging device according to claim 64, wherein said reset transistor is addressed by a reset line which is linear in said substrate.

66. (New) The imaging device according to claim 65, wherein said reset line is formed of a material selected from the group consisting of doped polysilicon, metals and refractory metal silicides.

67. (New) The imaging device according to claim 64, further comprising a row select transistor responsive to a row select signal to activate said imaging device.

68. (New) An imager comprising:

a plurality of pixel cells having a generally S-shaped active sensor area, the cells being arranged into an array of rows and columns, each pixel cell being operable to generate a voltage at a diffusion node corresponding to detected light intensity by the sensor, wherein two cells in a row share a common column line for addressing said pixel cell and the pixel cells in the row that share the common column line are alternatively addressed by respective row select lines.

69. (New) The imager according to claim 68, further comprising:

a row select device connected to either an odd row select line or an even row select line respectively; and

a row decoder having a plurality of control lines connected to the pixel cells, each control line being connected to the cells in contact with a respective column, wherein the row decoder is operable to activate odd cells in said rows and even cells in said rows by said row select device.

70. (New) The imager according to claim 69, further comprising:

a reset device to reset the voltage of a diffusion node formed in the cells;

a transfer device to transfer charge from said pixel cells to said diffusion node; and

a plurality of output circuits respectively connected to a pixel cell, each output circuit being operable to store a voltage signal received from a respective pixel cell and to provide a sensor output signal.

71. (New) The imager according to claim 68, wherein said pixel cells include a photogate, a photodiode or a photoconductor in said active area.

72. (New) The imager according to claim 68, wherein said column line addressing two adjacent rows of pixel cells is linear in said substrate.

73. (New) The imager according to claim 70, wherein said reset device is addressed by a reset line which is linear in said substrate.

74. (New) The imager according to claim 69, wherein said row select device is addressed by a row select line which is linear in said substrate.

75. (New) A CMOS imager array comprising:

a plurality of CMOS imager pixels for generating an output signal from detected light and arranged in rows and columns in an array, at least one of said CMOS imager pixels having an active area having a diagonally-shaped component;

a plurality of column lines each connected to at least two adjacent pixels of a row in said array, said column lines being connected to output circuitry to output signals generated from detected light;

a plurality of odd row select lines orthogonal to said column lines to address odd pixels in said rows;

a plurality of even row select lines orthogonal to said column lines to address even pixels in said rows;

column drivers to address the pixels connected to said column lines;

row drivers to address the pixels through said odd row lines and said even row lines.

76. (New) The CMOS imager array according to claim 75, wherein said column line is linear in said array.

77. (New) The CMOS imager array according to claim 76, wherein said column line is formed of a metal.

78. (New) The CMOS imager array according to claim 75, wherein said odd row lines and said even row lines are linear in said array.

79. (New) The system according to claim 75, wherein said CMOS imager is part of a camera system, a scanner, a machine vision system, a vehicle navigation system or a video telephone system.